THAT WHICH IS CLAIMED IS:

1. Process for fabricating an integrated circuit, comprising a substrate of crystalline silicon and a gate formed on the substrate, in which:

- a single step of amorphizing a region of the substrate is carried out in order to obtain an amorphous silicon region;
- a step of implanting a dopant species in a subregion lying substantially within the said region of the substrate is carried out in order to form drain and source extensions; and
- a step of forming the source and drain at low temperature is carried out.

2. Process according to Claim 1, in which, after the implantation step, a spacer formation step is carried out.

3. Process according to Claim 1 or 2, in which, after the implantation step, a low-temperature annealing step is carried out.

4. Process according to any one of the preceding claims, in which the source and drain formation step includes a deep amorphization substep.

5. Process according to any one of the preceding claims, in which the source and drain formation step includes a dopant species implantation substep.

6. Process according to Claim 4 or 5, in which, after the deep amorphization step or the dopant

species implantation step, a silicon recrystallization substep is carried out.

7. Process according to Claim 2, in which the step of forming the spacers includes a low-temperature annealing substep.

8. Process according to Claim 2, in which an annealing step is carried out after formation of the spacers.

9. Process according to any one of the preceding claims, in which a step of forming pockets in the substrate is carried out, said pockets being doped with a dopant species having the opposite conductivity to that of the dopant species of the implantation step.

10. Process according to Claim 9, in which the step of forming the doped pockets takes place before the amorphization step.

11. Process according to Claim 9, in which the step of forming the doped pockets takes place after the amorphization step.

12. Process according to Claim 9 or 10, in which the step of forming the doped pockets takes place before the amorphization step and before the dopant species implantation step.

13. Process according to any one of the preceding claims, in which a step of forming the spacers is carried out after the dopant species implantation step.

14. Process according to any one of the preceding claims, in which a step of forming the spacers is carried out before the amorphization step.

15. Process according to any one of the preceding claims, in which the amorphization step takes place to a thickness of greater than 100 nanometers.

16. Process according to any one of the preceding claims, in which a source and drain implantation step is carried out after the amorphization step.

17. Process according to any one of the preceding claims, in which the source and drain formation step includes a low-temperature annealing step.

18. Process according to any one of the preceding claims, in which the amorphization step includes the implantation of electrically inactive heavy ions.

19. Process according to Claim 18, in which the heavy ions are chosen from silicon, germanium, argon, neon, zenon and krypton.

20. Process according to any one of the preceding claims, in which the dopant species implanted during the said implantation step is chosen from the following species: B^+, BF_2^+, In^+, As^+, P^+ and Sb^+.

21. Process according to any one of the

preceding claims, in which the temperature of the source and drain formation step is below 800°C.

22. Integrated circuit comprising at least one transistor obtained by the process according to one of Claims 1 to 21.

23. Integrated circuit according to Claim 22, characterized in that the gate length of the transistor, measured parallel to the length of the channel, is less than 180 nanometers.

24. Integrated circuit according to Claim 23, characterized in that the gate length of the transistor, measured parallel to the length of the channel, is less than 100 nanometers.